Claims

1. Method for switching on a power switch (S1, S2) arranged between capacitive elements (C1, DLC, B36),

characterized in that

at least one compensating element (L), by way of which equalizing currents can flow between elements (C1, B36, DLC) which are to be connected to one another and can decay before the power switch (S1, S2) is subsequently closed in a current-free and no-voltage situation, is connected in parallel to the switching contacts of the still open power switch (S1, S2).

2. Method according to Claim 1, characterized in that the parallel connection of the compensating element (L) with respect to the switch-on command (Um) for switching on the power switch (S1, S2) takes place delayed by a first delay time (T1).

3. Method according to Claim 1, characterized in that the switch-on of the power switch (S1, S2) takes place only after an equalizing current has decayed and only when a second delay time (T2) beginning with the switch-on command (Um) has elapsed.

4. Device for implementing the method according to one of Claims 1 to 3, characterized in that
the compensating element (L) is a choke which can be connected in parallel with the switching contacts of the still open power switch (S1, S2) by means of a further switch (S3),
a detection circuit (DTS) is provided which detects a current flowing between the (C1, DLC, B36) elements which are to be connected to one another, and

a control device (SG) is provided, by which the power switch (S1, S2) is closed as soon as no equalizing current flowing by way of the choke (L) is detected by the detection circuit.

5. Device according to Claim 4, characterized in that a resistor (R) is connected in series with the choke (L), which is the ohmic resistor of the choke or a real resistor.

6. Device according to Claim 4, characterized in that the detection circuit (DTS) is designed such that
a series circuit comprising a resistor (R1) and the emitter-collector path of a pnp transistor (Q1) branches off from the one connection (A) of the choke (L), and a series circuit comprising a resistor (R3) and the emitter-collector path of a pnp transistor (Q2) also branches off from the other connection point (B) of the choke (L),
the collectors of the two transistors (Q1, Q2) are connected to one another and by way of a series circuit comprising two resistors (R7 and R8) to ground (GND),
a series circuit comprising a diode (D1) conducting current to ground (GND) and a resistor R2 is located between the one connection point (A) and ground (GND), and a series circuit comprising a diode (D2) conducting current to ground (GND) and a resistor R4 is also located between the other connection point (B) and ground (GND),
the connection point between diode (D1) and resistor (R2) and the base of the pnp transistor (Q2) are connected by means of a resistor (R5), and likewise the connection point between diode (D2) and resistor (R4) and the base of the pnp transistor (Q1) are connected by means of a resistor (R5), and the connection point between the two resistors (R7 and R8) is connected to the base of an npn transistor (Q3) whose emitter is connected to ground (GND), and whose collector is connected on the one hand by way of a resistor (R9) to a supply voltage

(Vcc) , and is connected on the other hand to a terminal (Mess) of the control device (SG).

7. Device according to Claim 4, characterized in that the control device (SG)
has a first delay element (T1) which delays the parallel connection of the choke (L) to the open power switch (S1, S2) by a predefined first delay time (T1) starting from the switch-on command (Um), and
has a second delay element (T2) taking the form of a monoflop which permits the switch-on of the power switch (S1, S2) at the earliest after a second delay time (T2) has elapsed which is longer than the first delay time (T1) and starts running at the beginning of the switch-on command (Um).

8. Device according to Claim 4, characterized in that the switch-off of the power switch (S1, S2) takes place at the end of the switch-on command (Um).

9. Device according to one of Claims 4 to 8 for the alternative connection of a capacitive element (C1) to further elements (DLC, B36), characterized in that
the further switch (S3) is a changeover switch,
the first delay element (T1) is a dual-edge triggered delay element,
the second delay element (T2) takes the form of a dual-edge triggered monoflop, and
all power switches (S1, S2) are opened upon the appearance of the switch-on command (Um), which in this case is a changeover command.

10. Device according to one of Claims 4 to 9, characterized in that the power switches (S1 to S3) are relay-controlled switches.